DAN SHU

RF/MMWAVE SYSTEM ARCHITECT SAN JOSE, CA 95120 408-219-8739 (CELL), 408-809-4978 (HOME)

DETAILS

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HIGHLIGHTS

Seasoned RF Front End architect.

RF and mmWave system architect.

Low power architect for Qualcomm's WiFi reference design.

RF simulation for WiFi, BT, LAA, 5G NR-U, UWB coexistence, including antenna sharing and Rx desense solving.

Applied machine learning algorithm on modem SoC dynamic rail voltage scaling for power saving.

Data driven decision making: MSSQL and MySQL database experience with large engineering data analysis skill.

Software and tools: SystemVue, Matlab, ADS, HFSS, ISD, Spotfire, JMP, SPICE, Allegro, C++, Java, Python, Unix scripts, iperf, IxChariot etc.

PROFILE

15+ years of communication industry experience building up capability and capacity focusing on delivering results. True innovator with strong industry connections. A passionate linchpin who can quickly connect dots and identify new opportunities.

EMPLOYMENT HISTORY

Principal Engineer, Coherent Application at MACOM, Santa Clara
April 2023 — June 2023

Reported to Metro and Longhorn business unit, worked on 128G coherent products.

- Simulated coherent system QAM64 performance (256G/s) by SystemVue.
- Built up process of visualizing ADS large quantity dataset (>10k .S4P files)
- Characterized OTP and TIA by hands-on created Python based tester.

SENIOR STAFF, Connectivity Hardware System Architect at Qualcomm Atheros, San Jose
October 2014 — March 2023

Owner of Front-End Module (FEM) qualification process. Owner of Power, thermal KPIs. Owner of reference design RF co-existing FEM KPIs.

Drove Mobile RF Front End (RFFE) design, qualification for next generation WiFi7, BT, UWB, and 5G NR-U coexist.

- Conducted line-up analysis over multi-stage Tx/Rx look up tables.
- Successfully simulated and predicted WiFi7 MLO 5/6G bands co-exist mode Lo spur 2nd order mixer effects caused Rx desense.
- Worked on linear/nonlinear/Doherty PA with DPD, memory DPD, CFR, ET, APT, multi modes PA/LNA for low power, cost effective FEM module designs.
- Hands-on validated, characterized FEMs for EVM, drooping, Mask, ACP, IIP2/3, NF, power efficiency etc. over process, voltage, and temperature.
- I am the one who defined Wi-Fi 6E/7 LNA KPIs 3 years ahead of time.

Partner with Qualcomm's different technology teams to design innovative digital enhancements to wireless products.

- Brought up 11be/WiFi7 waveforms from Matlab/SystemVue simulation to Lab bench validation for compensating various RF impairments.
- Researched PA drooping compensation methods from both silicon process and system baseband.

Worked on 4 categories of battery driven mobile system-level low power design. Owner of power, thermal, throughput, latency KPIs over process, voltage, and temperature.

- Lower voltage, current, leakage and frequency.
- Shorten the SoC circuit activity time such as power collapse, clock gate etc.
- Balance trade-offs on RF coverage, throughput, and power per Day-of-Use cases.
- Use CSMA/CA based approach to lower the system wake-up frequency.

Invented mobile SoC dynamic voltage control algorithm for power saving and throughput improvement based on multivariate machine learning models.

- Used multivariate machine learning models to calculate the polynomial functions SoC Vmin vs. SoC Process, Tj, and Throughput.
- Model results have been validated on three generations of SoC designs.

Maintaining the pace of per year learning/creating 2 new things in addition to daily work.

- 2023, Built MSSQL database and implemented off-the-shelf DPD solution.
- 2022, Invented sinewave drooping characterization method and enabled SystemVue simulation platform for complex RF co-exist simulation.
- 2021, Completed 11be compressed PAPR waveform EVM analysis and physically verified 320M BW 11be waveform before SoC RTL releasing.
- 2020, Applied multivariate machine learning models to the mobile soc dynamic power rail voltage control algorithm as power saving method and promoted the Wi-Fi 6E FEM golden standard over all FEM vendors.
- 2019, Invented mobile reference power estimation tool for customers and maintained power thermal KPIs.
- 2018, Invented access point power estimation tool for customers and created new FEM module evaluation platform.
- 2017 and before, Architected the 11be FTM DVT solutions and started mission mode performance vs. power evaluation task.

PRINCIPAL ENGINEER, ATE ARCHITECT at Broadcom, Santa Clara
March 2013 — September 2014

Reported to network organization and bought SerDes ATE test for MIPS CPUs and 25GB Switch IC.

- Solved Broadcom IC backend operation challenges after merged with Netlogic's multi core server CPU business.
- Solved 10G, 25G Serdes ATE characterization and mass production test challenge for 144 lanes switch chip.

I/O CONSULTANT (CONTRACT) at AMD, Markham, Canada
November 2011 — October 2012

Reported to Advantest Test Characterization organization with responsibility for leading complex characterization SerDes ATE solution for APU, GPU, CPU line.

- Solved PCIE Gen3(8G/s) and GDDR5 ATE test challenges for GPU/APU.

PRINCIPAL ENGINEER at Gennum Corp/Semtech, Burlington, Ontario, Canada
May 2004 — October 2011

Reported to Directors and Sr. VPs with responsibility for leading bare die and final test backend business.

- Led a task force to deliver the 1st generation Thunderbolt cable drivers (CDRs and EQs) project for the Apple Mac Computer.
- Built 26.5GHz BW Optical Domain lab for ROSA/TOSA/TIA/Laser Driver.

EDUCATION

Bachelor degree in Electronic Engineering, major in radio technology, Xi'an Jiaotong University, Xi'an, China

Post graduate studies, major in digital signal process. On leave without completing the degree, University of Electronic Science and Technology of China, Chengdu, China

COURSES

Java, online 2022

Regression Models, Coursera Johns Hopkins online 2015

Statistical Inference, Coursera Johns Hopkins online course 2015

Machine Learning, Stanford online course 2014

Introduction To Databases, Stanford online course 2014